The complete FETishizator V2.2

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After having done some elementary investigations for the late project of Mr. Lukasz Fikus – to find a method of matching and amplifying the output signal of a DAC with solid state products – I found a proper way to achieve a tube-like sound, which cannot be determined easily from that of real glass tubes.

The background for this project was, that for a non-tube version of his highly acclaimed "Lampizator" there would be no need for an anode-voltage DC-supply and there would be no tube-heater consumption. All in all, we could spare a separate DC-supply.

I sent my opinions to Lukasz and after he tried my quick applied hand drawings and published them on his website, I found, that there are some mistakes in his schematic drawings (only evident in the first publication, some days later corrected!). Because my hand drawings based only on a computer designed circuit, I made my own real life experiments and designed a complete stage including a "quiet DC-supply". There were some problems with crosstalk.

To make the real McCoy complete, I also designed a PCB, for to make the building of this stage easy – even ready for beginners.

About sound:

During my experiments I found out, that the MOSFET cathode follower (Q_3) in my schematic is essentially necessary, if you want this tube-like, nasty triode sound. JFETs have the belonging, that they sound just like pentodes in triode mode (a little bit crispier than a triode, but with the same distortion characteristics). This leads from the fact, that the control grid of a JFET is more high-resistant than that of a triode and the output characteristics of the JFET show more that of a current source. The distortion products are nearly the same (almost only k_2 and k_4), which will guaranty this triode sound. To reduce this typical crispy sound, a small capacity should be brought into the circuit. This is done by using a small signal MOSFET as a cathode-follower. It has also the advantage, that the output of the circuitry has only some few tens of Ohms.

The schematic of Lukasz at his homepage:

The biggest mistake in his first schematic (now corrected by a liner note!) was the fact, that it showed a BF245B and he coupled it with surrounding elements, normally used for a BF245A. This would lead to a drain starvation effect and I would be highly surprised, if Lukasz found the sound as fabulous as he wrote.

The correct schematic is enclosed to this article. Please do not try to substitute the original JFET in this circuitry by any other type. I tried some other types and found that this is not so good an idea - reflected on sound.

The complete FETishizator:

I have to say, that I am not so happy with the name "FETishizator", so I call it "FET_CDout" in my papers. But I respect Lukasz's choice, so it shall stay, anyhow …

OK now - my schematic <FET_CDout.pdf> shows a circuitry, which is very similar, because it almost shows my original hand drawing:

I used a BF245A, because the maximum input voltage (leading from +4mA of the current output DAC-TDA1541) will be only 400mV$_{pp}$, if used with the input resistor R_2 = 100Ω (4mA*100Ω = 400mV).

The gate/source voltage of the BF245A is typically 1V at 1mA drain-current. Digitally Null output of the DAC will result in +2mA output current, which will reflect an input voltage of the JFET of +200mV. Full scale output of the DAC will result in – positive half-wave – +400mVDC (4mA * 100Ω), while - negative half-wave – in 0VDC; all peak to peak AC - seen as DC-voltage.

So we can presume a Null input voltage of +200mV as our design point. If the BF245A had 0V at its gate, it would show a drain current of 1mA, if we put a 1kΩ resistor into the source path. Because we have +200mV as design point we have to raise the value something to around 1200Ω to achieve the same drain current. JFETs are at their best performance at this 1mA drain-current, so do not change this value!

The drain resistor R_5 (5k6) has to settle half the remaining supply voltage across it, to give fully symmetrical operation.

In my given example, I presume a supply voltage (L/R_B+) of +12VDC. So we have to lower this value by 1,2V (the gate/source voltage) => 10,8V and then we have to divide it by 2 => 5,4V. 5,4V / 1mA leads to 5,4kΩ. The closest value is 5k6, which is close enough for our circuitry. The common formula reads:

$$R_5 = \frac{(V_{B+} - V_{GS})}{2 * I_D}$$

Note:

*You could improve the performance of this circuit, if you raised the B+ voltage until close to +30V (breakdown voltage of any BF245), but be sure, **never** to exceed this value! Use the above formula to make the needed dimensioning! Keep proper spares in your calculation! If VCC is close to +30VDC, a value of 12k … 15k (R5) will be a good point to start with. R15, R18 should settle to 5k6 each.*

JFET breakdown will never destroy the DAC, because its gate is isolated from the channel and even channel (source/drain) breakdown will be held-back by the “quiet DC-supply” circuit. But you had to replace the JFET, because it would not operate any more!

Since the current through R_3 (1200Ω) will cause a current feedback, we have to bypass this resistor by some capacitance. As I wrote in my “Music Angel Mod article”, bigger electrolytic caps show an immeasurable phase problem, we have to bypass also with foil capacitors (C_4, C_5, C_6). By this means, the current-feedback only exists for DC (for a stable DC operating point) but not for AC current. The AC amplification will therefore be much higher. The common formula for the dimensioning of caps reads:

$$C_{RS} = \frac{1}{2 * \pi * f_u * R_S}$$

You should settle f_u to about ≤5Hz to get satisfactory results. This formula can also be used for all input and output caps! Only substitute input resistance or output resistance instead of R_s.

At the drain of the JFET the MOSFET (BS170) is coupled. It cannot do any good or bad to the overall audible sound, it matches only impedance while it reduces high frequent dirt in the signal (above 0,5MHz) by its gate capacitance.

Please note: Tubes do the same by their grid- and Miller-capacitance!!!

The "quiet DC-supply" - flanking each audio channel - is consisting of a very high gain Darlington transistor in connection with some passive parts, which all in all form a "gyrator". The function of this stage is very versatile and can be seen like a choke, built of "sand". The input voltage (VCC) may be as high as 120VDC if you use the mentioned BD651. Not all parts on the schematic drawing are used in common for all applications. I enclosed four typical dimensionings for VCC => ~ 12V, 15 … 20V, 24V … 30V, bigger (50V) in the back of this article. The BD651 stabilizes the supply voltage, while it decouples both audio channels to a maximum and while it also smoothes B+ like a serial choke.

Theory tells, if you connect a cap to the inverting input (here: transistor base) of a current amplifying part, the complete circuit acts like an inductance. Big bargain in this small and sophisticated circuit!

I also enclosed the copper layout <FET_CDout_Cu.pdf> in real life size (1:1), from which you can easily make your on PCBs. The stuffing drawing is named <FET_CDout_top.pdf> and also enclosed.

Possible and/or some needed mods in the audio circuit:

- For use with the above mentioned current-output DACs (TDA1541 e.g.) the input caps C_{25} and C_{26} are not used. They are substituted by wire bridges.
- If you have a voltage output DAC, you should have a look at the manufacturer's datasheet of the sample. If the output voltage is smaller than $400mV_{pp}$ (peak to peak), you can stay with the given schematic and you have to use the above mentioned input capacitors, if the output voltage is not symmetrical (pure AC). See the above formula for dimensioning of C_{25}. Input resistor R_2 should be about 10 times the value of the specified inner resistance, mentioned in the datasheet as "output resistance" f.e.

  Some math:

  Datasheet says V_{out} is < $400mV_{pp}$, while R_{out} is < 10kΩ =>

  $R_2 \geq 100k\Omega$ and according to the above formula $C_{25} = \frac{1}{2 * \pi * f_u * R_2}$ =>>

  C_{25} = 1/(2*PI*5*100.000) ➔ 318nF ➔ you can use 0,33µF or bigger.

- If the output voltage is bigger than 400mV_{pp} but smaller than 2V_{pp}, you should use a BF245C and also change R_3 to 3k9.
- If the output voltage is bigger than 2V_{pp}, you should use a BF245C and also change R_3 to 3k9. Additionally you have to divide the output voltage of the DAC in a way to get about 2V_{pp}.

Possible and/or some needed mods in the gyrator circuit:

- VCC is around +12V:

  R_8 = 10Ω; R_9 = 10Ω; R_{11} = omitted; D_1 = omitted
- VCC is +15 … 20V:

  R_8 = 10Ω; R_9 = 2k2; R_{11} = 4k7; D_1 = omitted
- VCC is +24V … 30V:

  R_8 = 10Ω; R_9 = 3k9; R_{11} = omitted; D_1 = 12V-Zener (e.g. BZX55C12)
- VCC is bigger (e.g. +50V):

  R_8 = 1k5; R_9 = 3k9; R_{11} = omitted; D_1 = 12V-Zener (e.g. BZX55C12)

Some hints on mounting and wiring:

- Keep wires from DAC to the PCB as short as possible.
- Always look for the highest DC voltage inside your CD player. It is the best for VCC supply!
- The PCB is not subject to EMI/RFI catching (tested!) because of its proper copper ground-plane-design. Thus in fact try to keep it some inches away from mains transformers and digital chips. In serious cases, you had to insert the PCB into a shielding metal case.
- Only connect GND one (1) time to the remaining circuitry of the player. Try to find the best/quietest point for this connection. Use an AC mV-meter at the audio output to determine this connecting point!!!

If you use this circuit with solid state amplifiers, capable of very high upper frequency limits (>500kHz -3dB), you should not use it without a radio frequency trap (AM-coil) in series with the audio output. Tube power-amps are generally not critical.

Caution: This circuit has no built-in trap for the residual radio frequency dirt of the D/A conversion, which could become almost as high as 50% of the maximum audio signal. It is designed and built along the ideas of Lukasz's "Lampizator". It could damage your valuable solid state amps and tweeters!!!

Although I could not find this fact during my in-circuit tests, you had to be aware of it!

BF245 have a transition frequency of about 700MHz! The MOSFET lowers this particular value a lot, but in any case – be careful!

You will not hear it first moment, but your amps and tweeters will burn after all!!!

APPENDIX:

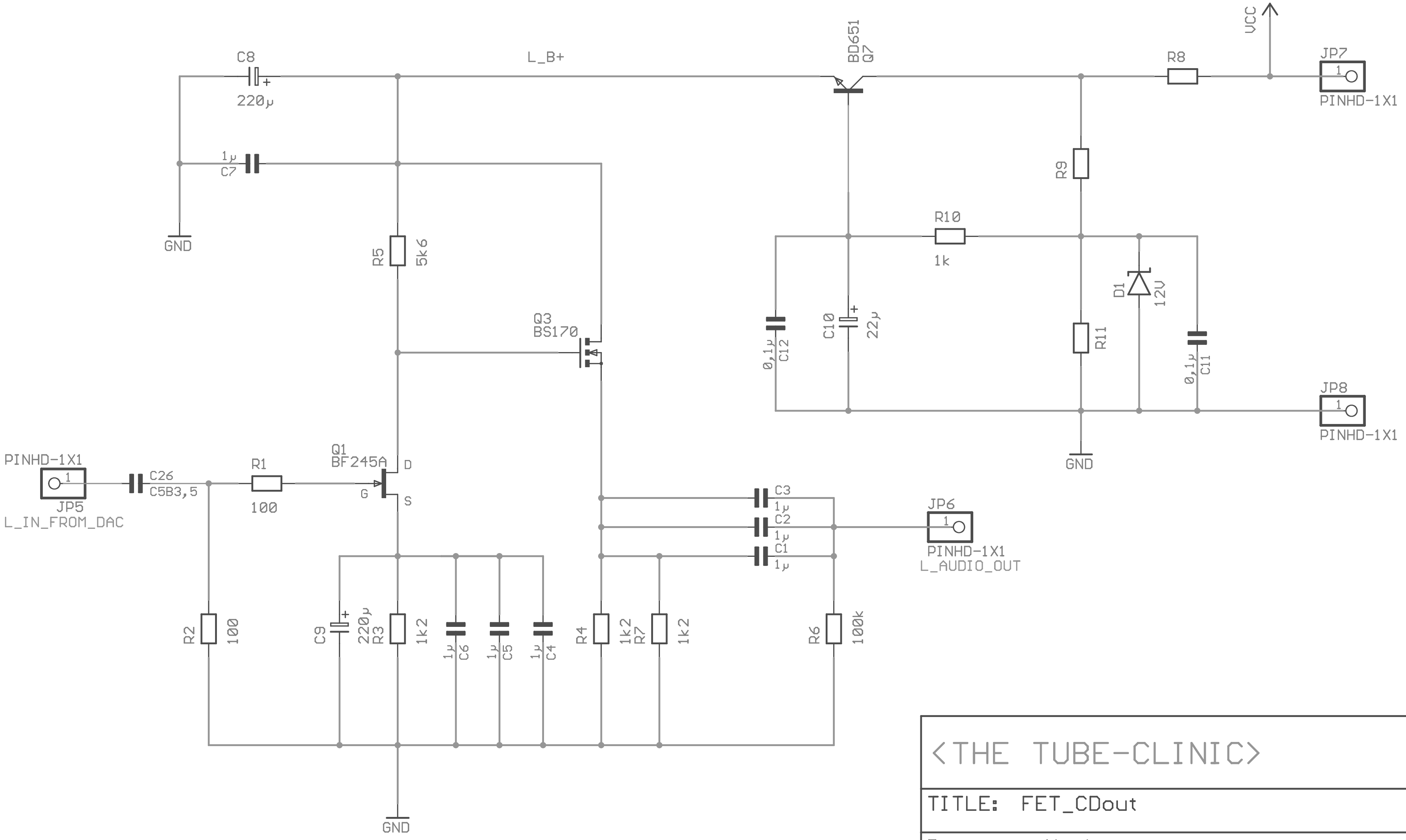
Design example for the widely used TDA1541:

Datasheet values:		**Your design values:**
Current output(pin 6, 25):		
I_{out} (at pos. full scale) I_{out} (at dig. Null) I_{out} (at neg. full scale)	+4mA +2mA 0mA	C_{25} = omitted; R_2 = 100Ω (V_{in} = +200mV_{pp}); output is designed for short circuit use! R_3 = 1k2; Q_1 = BF245A

Design example for the PCM61:

Datasheet values:		**Your design values:**
Voltage output (pin 9):		
V_{out} (at full scale)	±3V	In the place of C_{25} => 10k (C_{25} omitted); R_2 = 2k2 (V_{in} = 1082mV_{pp}); R_3 = 3k9; Q_1 = BF245C
I_{out} Output impedance	±2mA 0,1Ω	Do not care!
Current output(pin 13):		
I_{out} (at full scale) Output impedance	±1mA 1,2kΩ	C_{25} = omitted; R_2 = 150Ω (V_{in} = 300mV_{pp}); output is designed for short circuit use! R_3 = 1k; Q_1 = BF245A

For best audio results, you should always use the current output !!!



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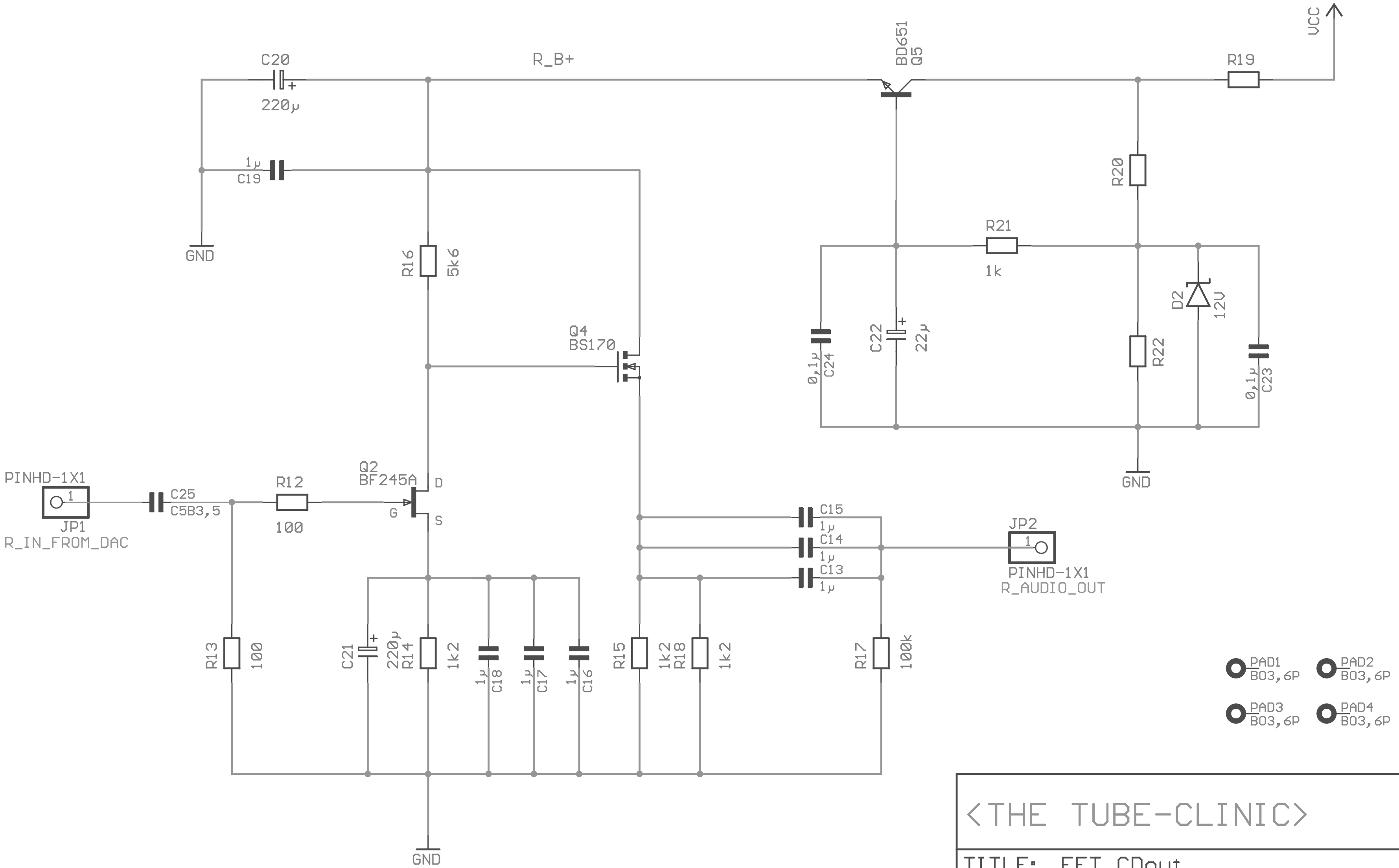

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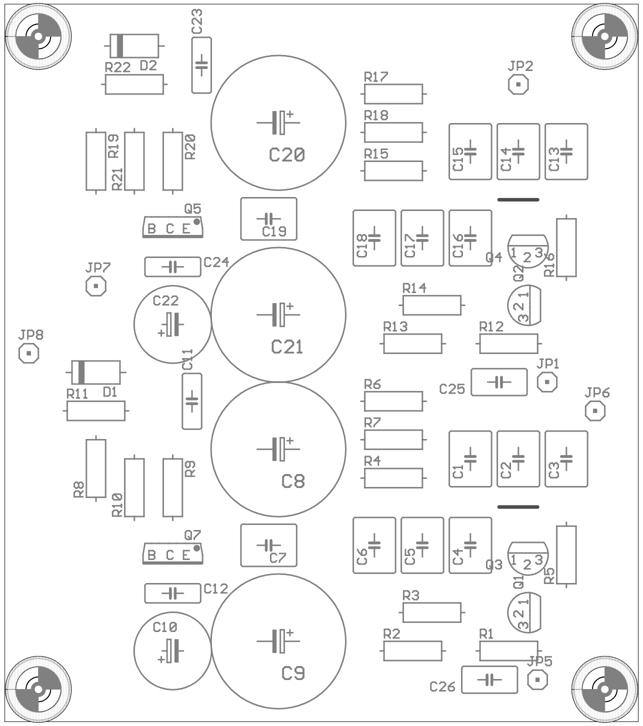
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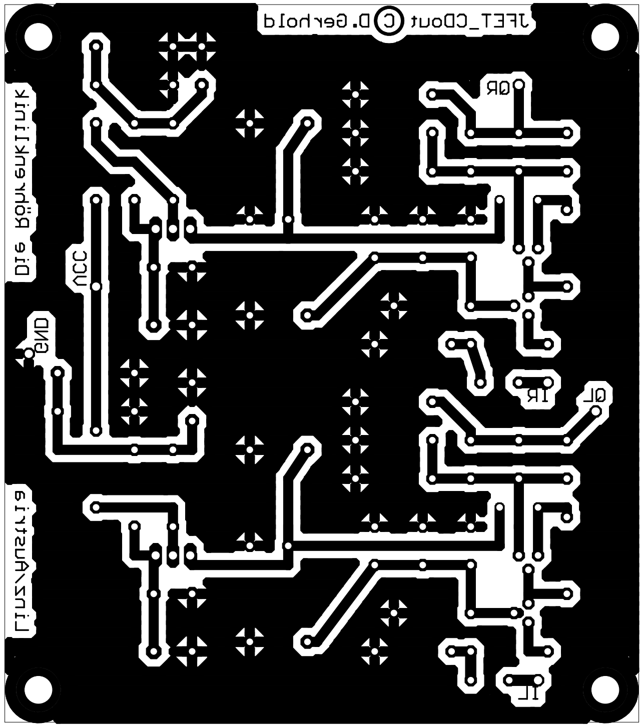

JFET_CDout © D.Gerhold
Die Röhrenklinik
Linz/Austria
VCC
GND
QR
IR
QL
IL

DATA SHEET

BF245A; BF245B; BF245C
N-channel silicon field-effect transistors

Product specification
Supersedes data of April 1995
File under Discrete Semiconductors, SC07

1996 Jul 30

Philips Semiconductors

PHILIPS

N-channel silicon field-effect transistors | BF245A; BF245B; BF245C

FEATURES

- Interchangeability of drain and source connections
- Frequencies up to 700 MHz.

APPLICATIONS

- LF, HF and DC amplifiers.

DESCRIPTION

General purpose N-channel symmetrical junction field-effect transistors in a plastic TO-92 variant package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	d	drain
2	s	source
3	g	gate

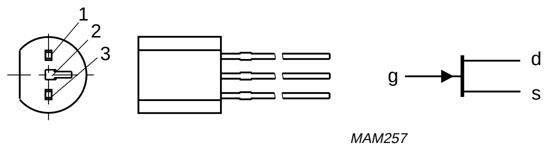


Fig.1 Simplified outline (TO-92 variant) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	±30	V
V_{GSoff}	gate-source cut-off voltage	I_D = 10 nA; V_{DS} = 15 V	–0.25	–	–8	V
V_{GSO}	gate-source voltage	open drain	–	–	–30	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0				
	BF245A		2	–	6.5	mA
	BF245B		6	–	15	mA
	BF245C		12	–	25	mA
P_{tot}	total power dissipation	T_{amb} = 75 °C	–	–	300	mW
$\|y_{fs}\|$	forward transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	3	–	6.5	mS
C_{rs}	reverse transfer capacitance	V_{DS} = 20 V; V_{GS} = –1 V; f = 1 MHz; T_{amb} = 25 °C	–	1.1	–	pF

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	±30	V
V_{GDO}	gate-drain voltage	open source	–	–30	V
V_{GSO}	gate-source voltage	open drain	–	–30	V
I_D	drain current		–	25	mA
I_G	gate current		–	10	mA
P_{tot}	total power dissipation	up to T_{amb} = 75 °C;	–	300	mW
		up to T_{amb} = 90 °C; note 1	–	300	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board, minimum lead length 3 mm, mounting pad for drain lead minimum 10 mm × 10 mm.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	250	K/W
	thermal resistance from junction to ambient		200	K/W

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)GSS}$	gate-source breakdown voltage	I_G = –1 µA; V_{DS} = 0	–30	–	V
V_{GSoff}	gate-source cut-off voltage	I_D = 10 nA; V_{DS} = 15 V	–0.25	–8.0	V
V_{GS}	gate-source voltage	I_D = 200 µA; V_{DS} = 15 V			
	BF245A		–0.4	–2.2	V
	BF245B		–1.6	–3.8	V
	BF245C		–3.2	–7.5	V
I_{DSS}	drain current	V_{DS} = 15 V; V_{GS} = 0; note 1			
	BF245A		2	6.5	mA
	BF245B		6	15	mA
	BF245C		12	25	mA
I_{GSS}	gate cut-off current	V_{GS} = –20 V; V_{DS} = 0	–	–5	nA
		V_{GS} = –20 V; V_{DS} = 0; T_j = 125 °C	–	–0.5	µA

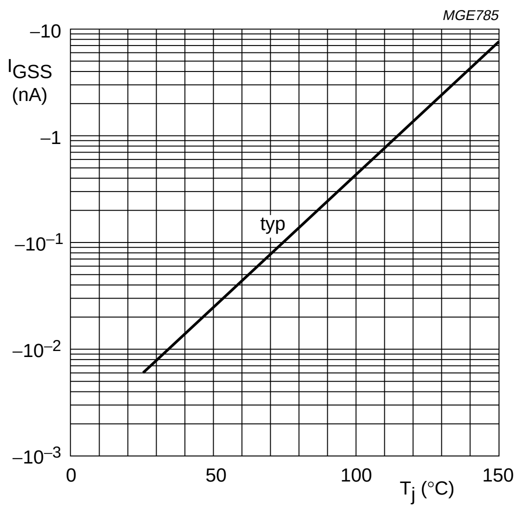
Note

1. Measured under pulse conditions: t_p = 300 µs; δ ≤ 0.02.

DYNAMIC CHARACTERISTICS

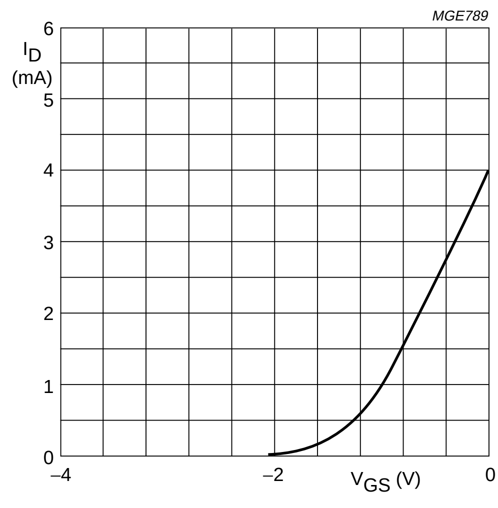
Common source; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{is}	input capacitance	V_{DS} = 20 V; V_{GS} = –1 V; f = 1 MHz	–	4	–	pF
C_{rs}	reverse transfer capacitance	V_{DS} = 20 V; V_{GS} = –1 V; f = 1 MHz	–	1.1	–	pF
C_{os}	output capacitance	V_{DS} = 20 V; V_{GS} = –1 V; f = 1 MHz	–	1.6	–	pF
g_{is}	input conductance	V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	250	–	µS
g_{os}	output conductance	V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	40	–	µS
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	3	–	6.5	mS
		V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	6	–	mS
$\lvert y_{rs} \rvert$	reverse transfer admittance	V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	–	1.4	–	mS
$\lvert y_{os} \rvert$	output admittance	V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	–	25	–	µS
f_{gfs}	cut-off frequency	V_{DS} = 15 V; V_{GS} = 0; g_{fs} = 0.7 of its value at 1 kHz	–	700	–	MHz
F	noise figure	V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz; R_G = 1 kΩ (common source); input tuned to minimum noise	–	1.5	–	dB



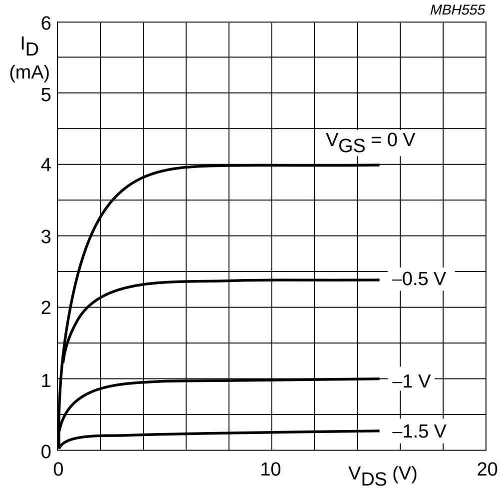
V_{DS} = 0; V_{GS} = –20 V.

Fig.2 Gate leakage current as a function of junction temperature; typical values.



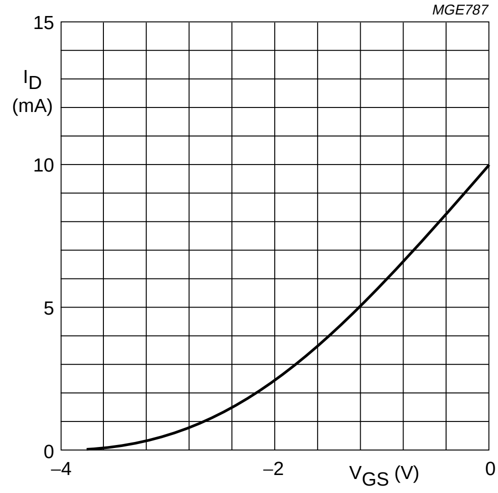
V_{DS} = 15 V; T_j = 25 °C.

Fig.3 Transfer characteristics for BF245A; typical values.



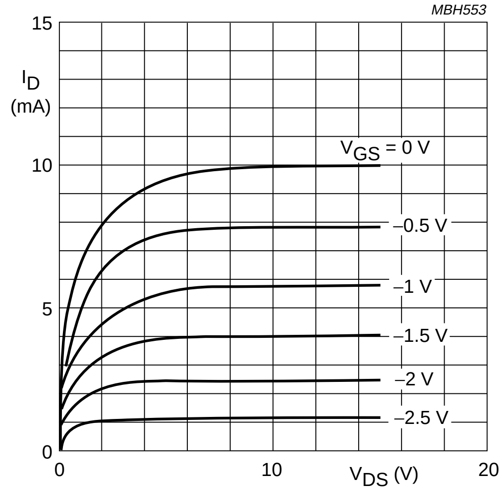
V_{DS} = 15 V; T_j = 25 °C.

Fig.4 Output characteristics for BF245A; typical values.



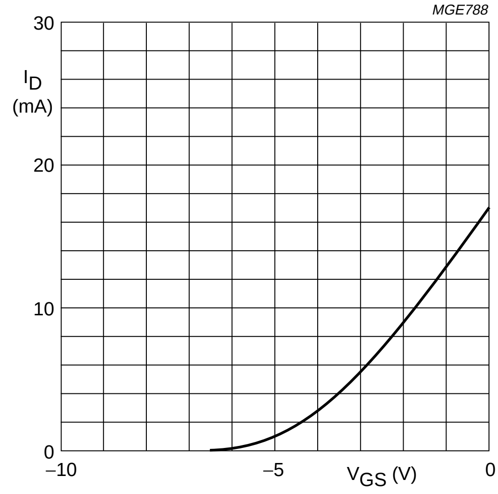
V_{DS} = 15 V; T_j = 25 °C.

Fig.5 Transfer characteristics for BF245B; typical values.



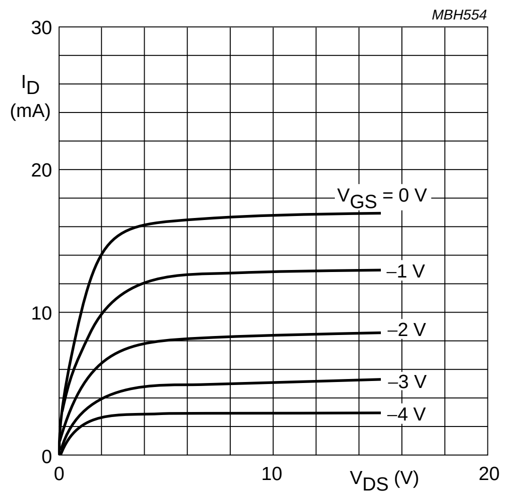
V_{DS} = 15 V; T_j = 25 °C.

Fig.6 Output characteristics for BF245B; typical values.



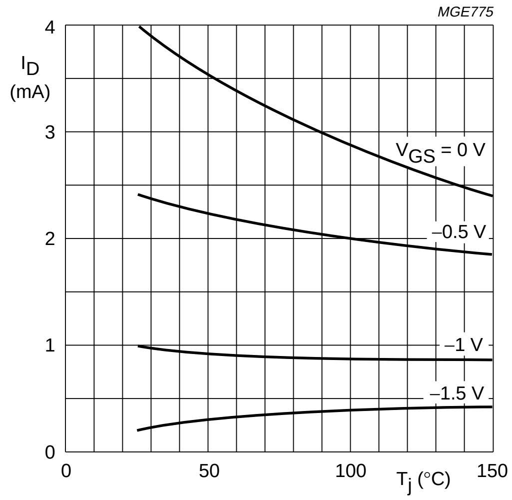
V_{DS} = 15 V; T_j = 25 °C.

Fig.7 Transfer characteristics for BF245C; typical values.



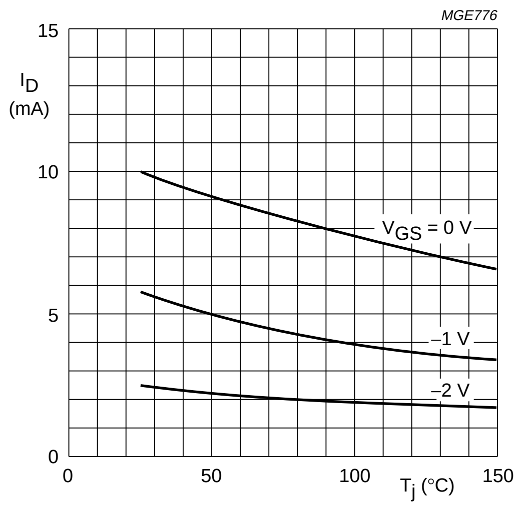
V_{DS} = 15 V; T_j = 25 °C.

Fig.8 Output characteristics for BF245C; typical values.



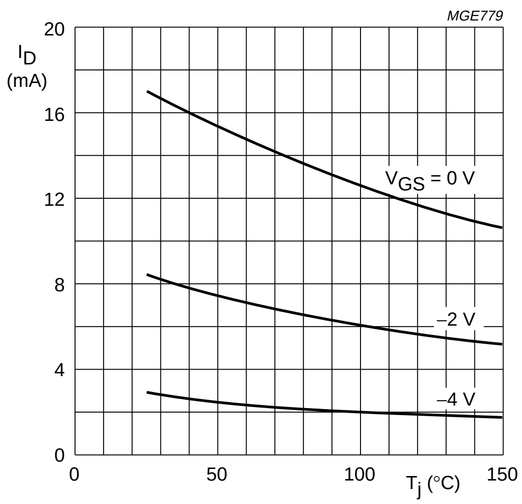
V_{DS} = 15 V.

Fig.9 Drain current as a function of junction temperature; typical values for BF245A.



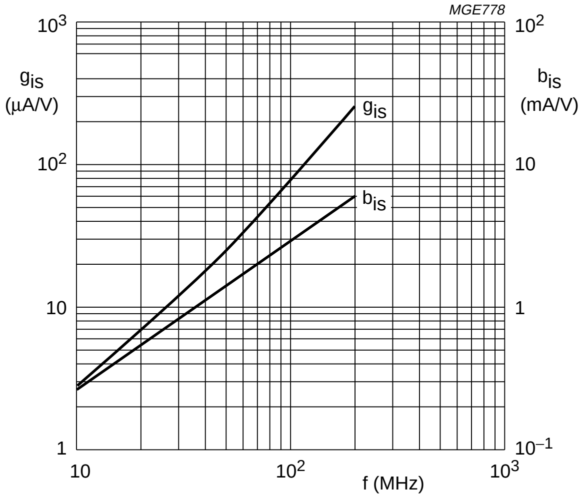
V_{DS} = 15 V.

Fig.10 Drain current as a function of junction temperature; typical values for BF245B.



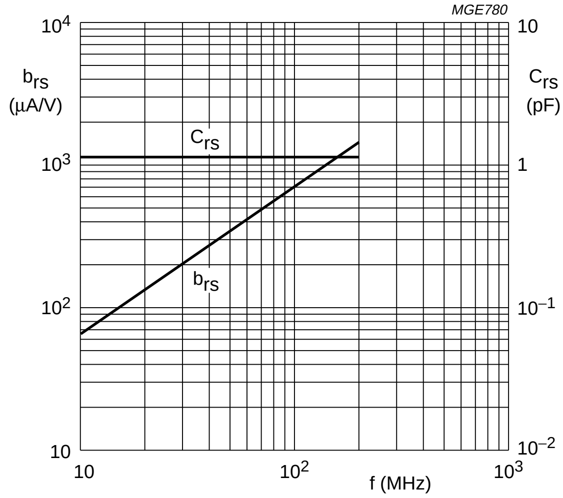
V_{DS} = 15 V.

Fig.11 Drain current as a function of junction temperature; typical values for BF245C.



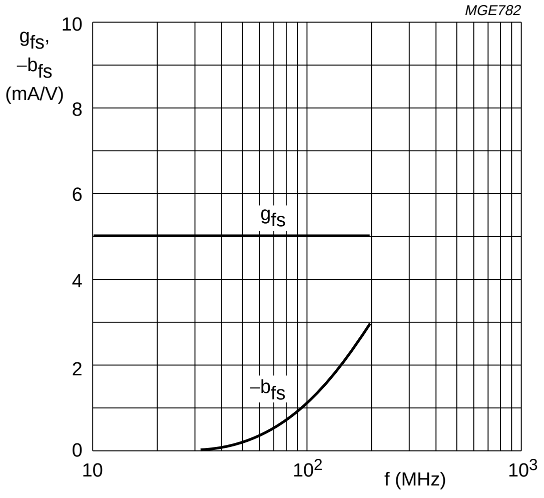
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.12 Input admittance; typical values.



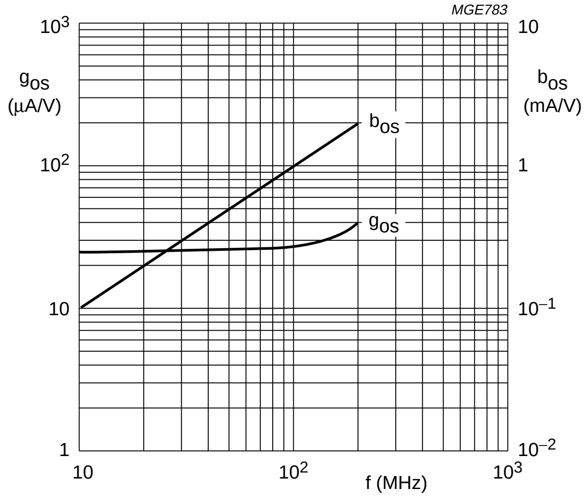
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.13 Common source reverse admittance as a function of frequency; typical values.



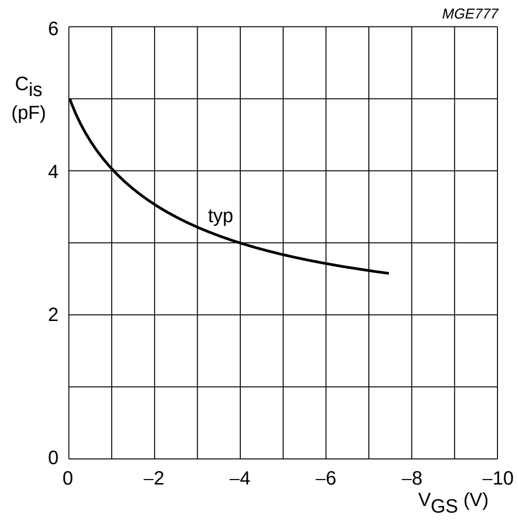
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.14 Common-source forward transfer admittance as a function of frequency; typical values.



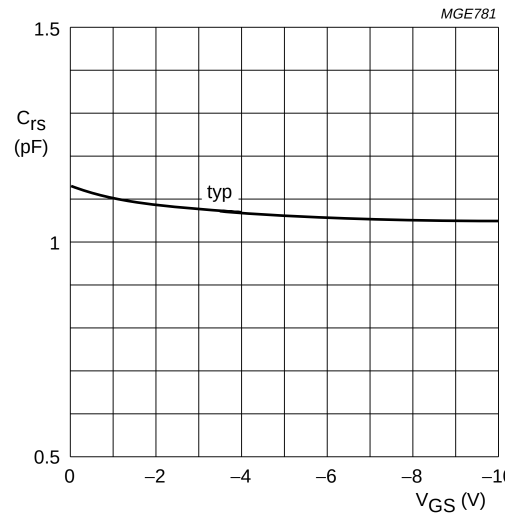
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C.

Fig.15 Common-source output admittance as a function of frequency; typical values.



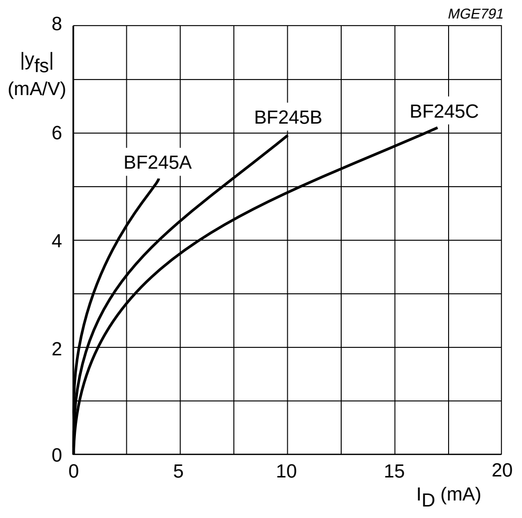
V_{DS} = 20 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.16 Input capacitance as a function of gate-source voltage; typical values.



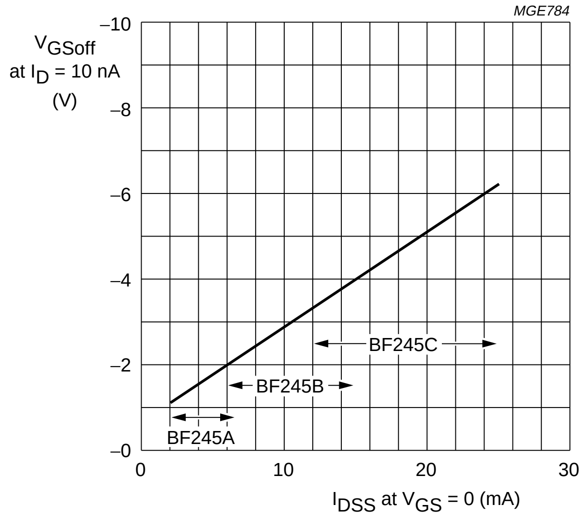
V_{DS} = 20 V; f = 1 MHz; T_{amb} = 25 °C.

Fig.17 Reverse transfer capacitance as a function of gate-source voltage; typical values.



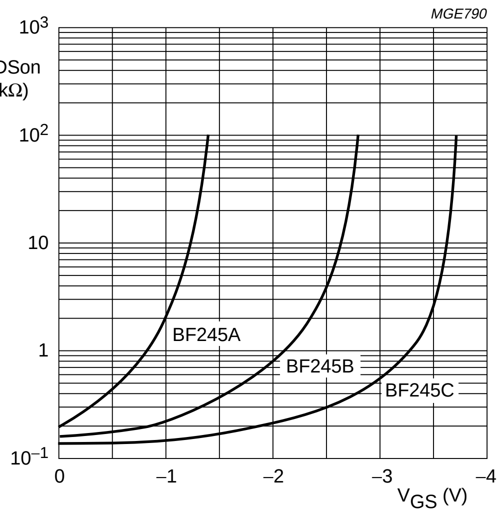
V_{DS} = 15 V; f = 1 kHz; T_{amb} = 25 °C.

Fig.18 Forward transfer admittance as a function of drain current; typical values.



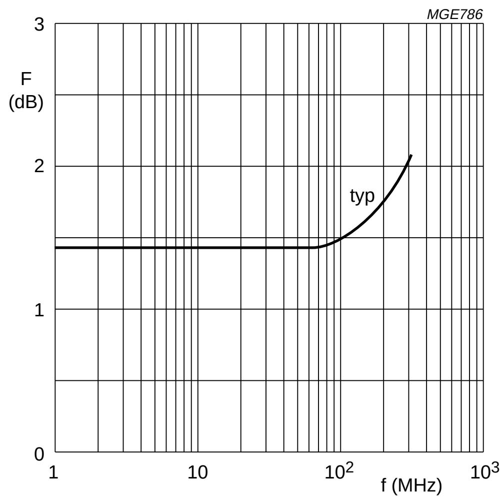
V_{DS} = 15 V; T_j = 25 °C.

Fig.19 Gate-source cut-off voltage as a function of drain current; typical values.



V_{DS} = 0; f = 1 kHz; T_{amb} = 25 °C.

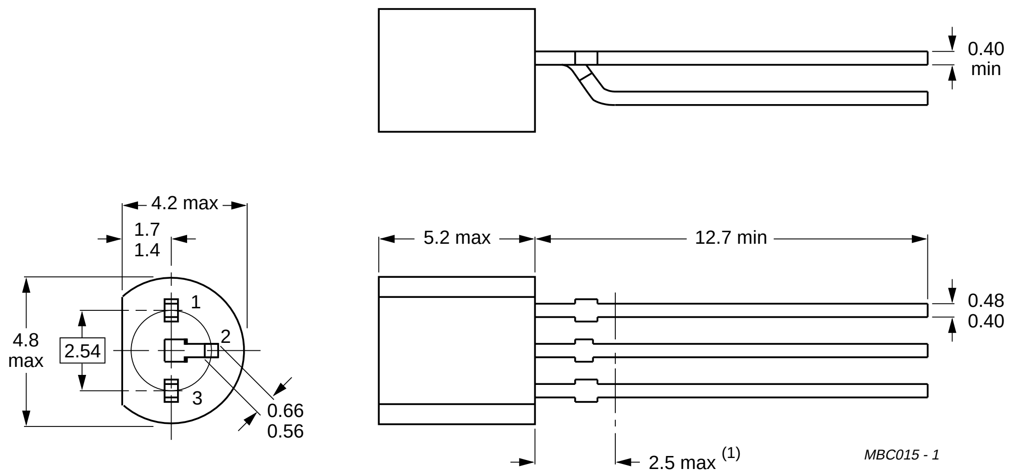
Fig.20 Drain-source on-state resistance as a function of gate-source voltage; typical values.



V_{DS} = 15 V; V_{GS} = 0; R_G = 1 kΩ; T_{amb} = 25 °C.
Input tuned to minimum noise.

Fig.21 Noise figure as a function of frequency; typical values.

PACKAGE OUTLINE



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled.

Fig.22 TO-92 variant.

DEFINITIONS

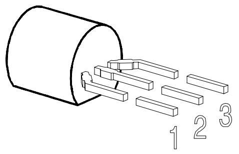
Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

SIPMOS ® Small-Signal Transistor

- N channel
- Enhancement mode
- Logic Level
- $V_{GS(th)}$ = 0.8...2.0V



Pin 1	Pin 2	Pin 3
S	G	D

Type	V_{DS}	I_D	$R_{DS(on)}$	Package	Marking
BS 170	60 V	0.3 A	5 Ω	TO-92	BS 170

Type	Ordering Code	Tape and Reel Information
BS 170	Q67000-S076	E6288

Maximum Ratings

Parameter	Symbol	Values	Unit
Drain source voltage	V_{DS}	60	V
Drain-gate voltage R_{GS} = 20 kΩ	V_{DGR}	60	
Gate source voltage	V_{GS}	± 14	
Gate-source peak voltage,aperiodic	V_{gs}	± 20	
Continuous drain current T_A = 25 °C	I_D	0.3	A
DC drain current, pulsed T_A = 25 °C	I_{Dpuls}	1.2	
Power dissipation T_A = 25 °C	P_{tot}	0.63	W

Maximum Ratings

Parameter	Symbol	Values	Unit
Chip or operating temperature	T_j	-55 ... + 150	°C
Storage temperature	T_{stg}	-55 ... + 150	
Thermal resistance, chip to ambient air [1)]	R_{thJA}	≤ 200	K/W
DIN humidity category, DIN 40 040		E	
IEC climatic category, DIN IEC 68-1		55 / 150 / 56	

Electrical Characteristics, at T_j = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain- source breakdown voltage V_{GS} = 0 V, I_D = 0.25 mA, T_j = 25 °C	$V_{(BR)DSS}$	60	-	-	V
Gate threshold voltage V_{GS}=$V_{DS,}$ I_D = 1 mA	$V_{GS(th)}$	0.8	1.4	2	
Zero gate voltage drain current V_{DS} = 60 V, V_{GS} = 0 V, T_j = 25 °C V_{DS} = 60 V, V_{GS} = 0 V, T_j = 125 °C	I_{DSS}	- -	0.05 -	0.5 5	µA
Gate-source leakage current V_{GS} = 20 V, V_{DS} = 0 V	I_{GSS}	-	1	10	nA
Drain-Source on-state resistance V_{GS} = 10 V, I_D = 0.2 A	$R_{DS(on)}$	-	2.5	5	Ω

Electrical Characteristics, at T_j = 25°C, unless otherwise specified

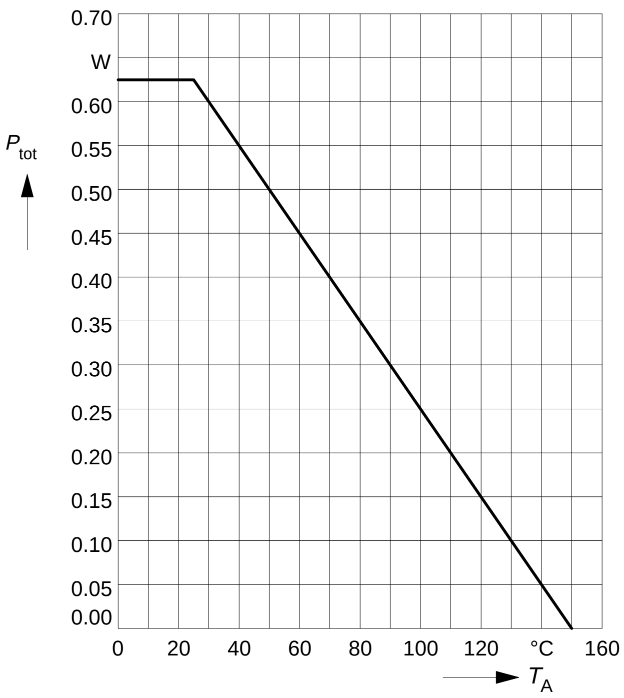
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Dynamic Characteristics					
Transconductance $V_{DS} \geq 2 * I_D * R_{DS(on)max}$, I_D = 0.2 A	g_{fs}	0.12	0.18	-	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	-	40	60	pF
Output capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{oss}	-	15	25	
Reverse transfer capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	-	5	10	
Turn-on delay time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 0.29 A R_G = 50 Ω	$t_{d(on)}$	-	5	8	ns
Rise time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 0.29 A R_G = 50 Ω	t_r	-	8	12	
Turn-off delay time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 0.29 A R_G = 50 Ω	$t_{d(off)}$	-	12	16	
Fall time V_{DD} = 30 V, V_{GS} = 10 V, I_D = 0.29 A R_G = 50 Ω	t_f	-	17	22	

Electrical Characteristics, at T_j = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Reverse Diode					
Inverse diode continuous forward current T_A = 25 °C	I_S	-	-	0.3	A
Inverse diode direct current,pulsed T_A = 25 °C	I_{SM}	-	-	1.2	
Inverse diode forward voltage V_{GS} = 0 V, I_F = 0.5 A	V_{SD}	-	0.9	1.2	V

Power dissipation

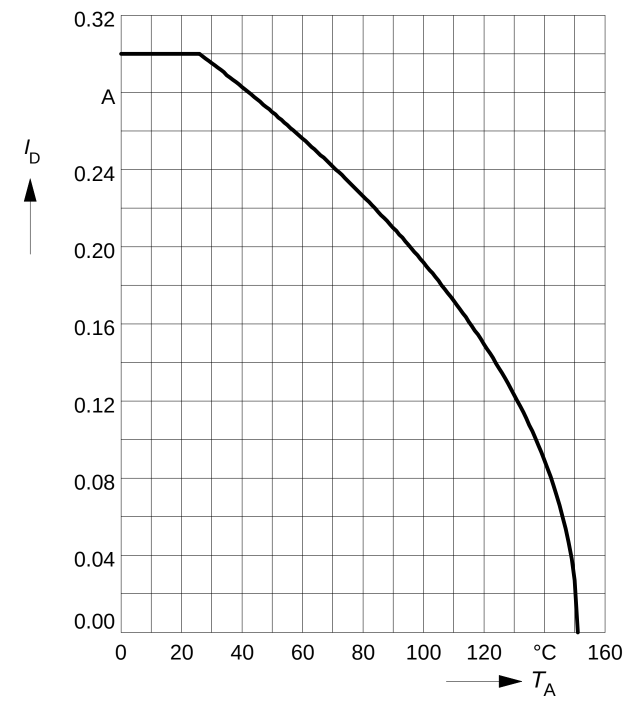
$P_{tot} = f(T_A)$



Drain current

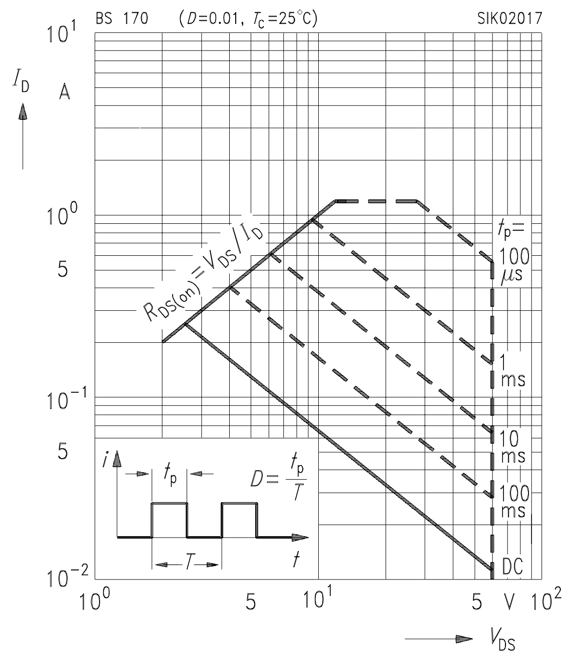
$I_D = f(T_A)$

parameter: $V_{GS} \geq 10$ V



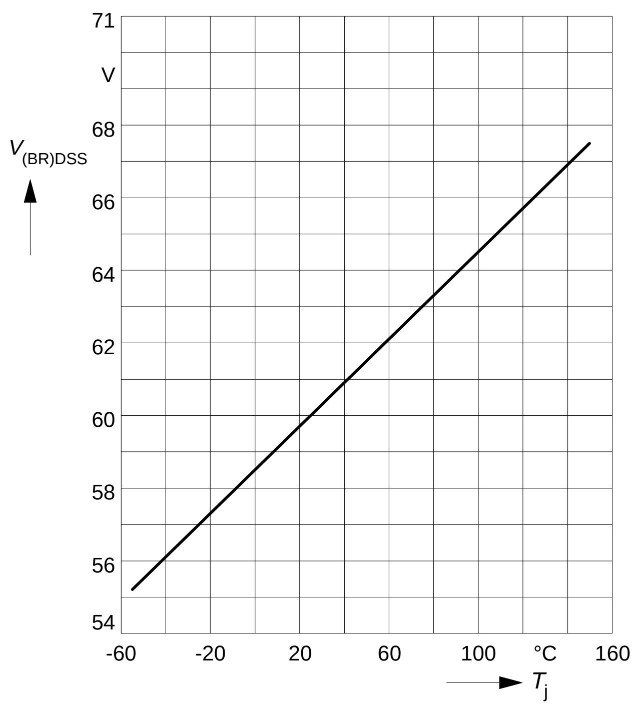
Safe operating area I_D=f(V_{DS})

parameter : D = 0.01, T_C=25°C

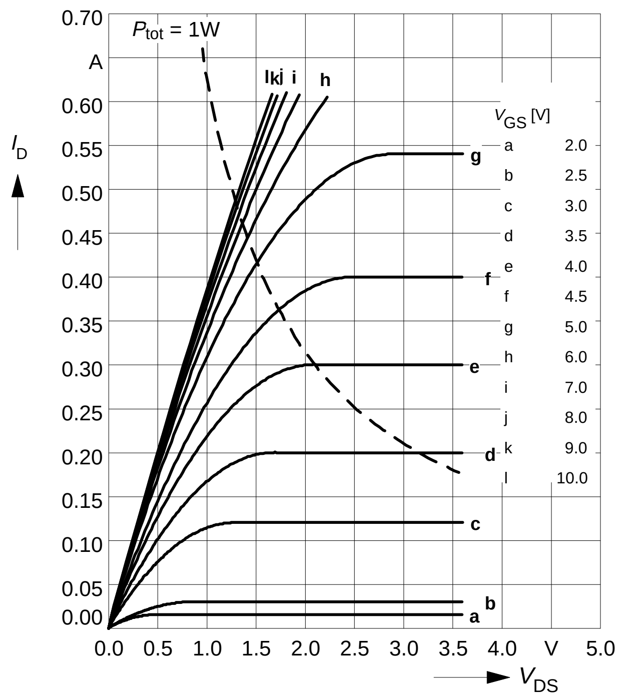


Drain-source breakdown voltage

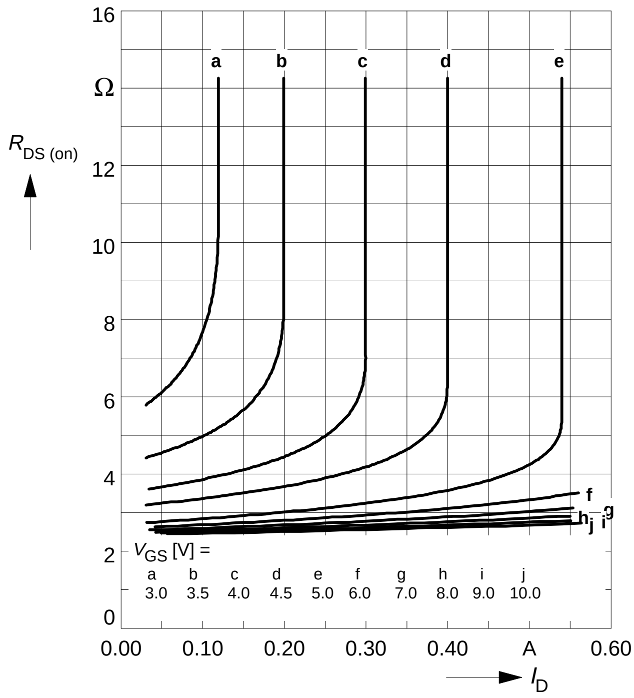
$V_{(BR)DSS} = f(T_j)$



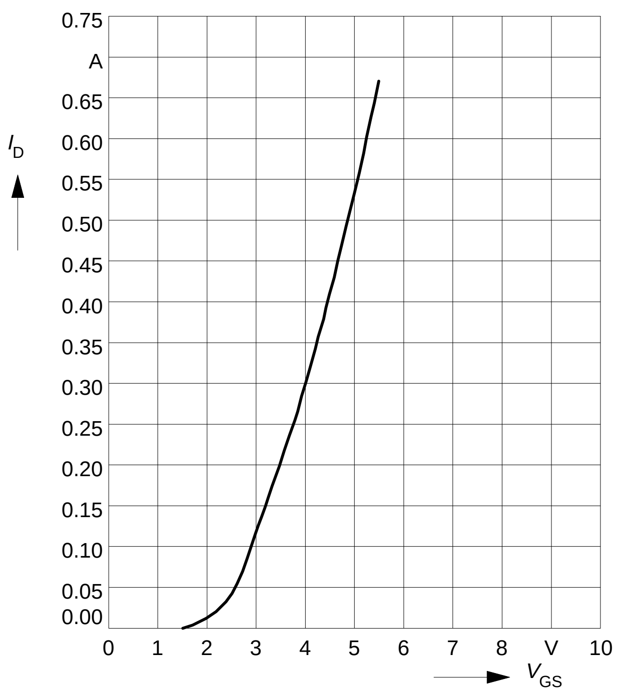
Typ. output characteristics
$I_D = f(V_{DS})$
parameter: t_p = 80 µs , T_j = 25 °C



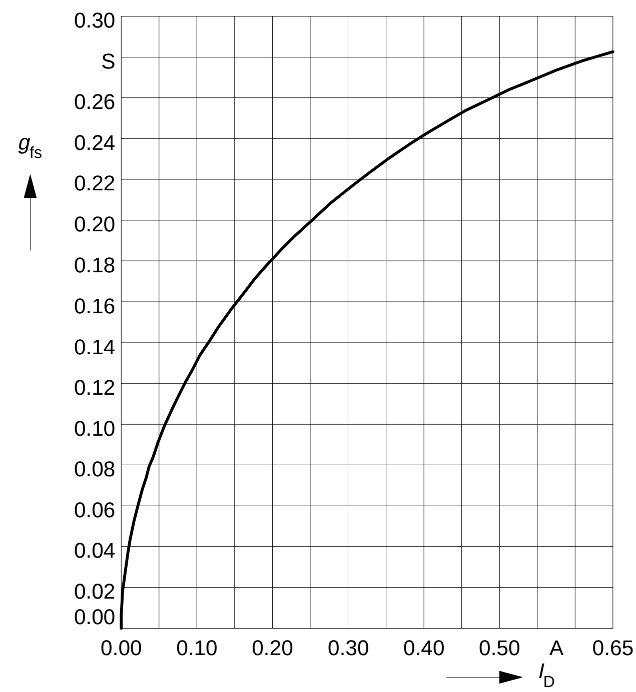
Typ. drain-source on-resistance
$R_{DS\ (on)} = f(I_D)$
parameter: t_p = 80 µs, T_j = 25 °C



Typ. transfer characteristics $I_D = f(V_{GS})$
parameter: t_p = 80 µs
$V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$



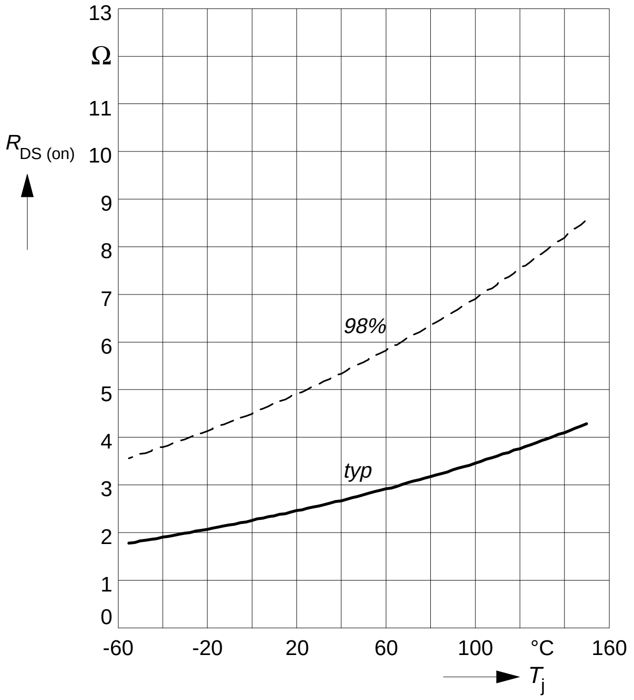
Typ. forward transconductance $g_{fs} = f(I_D)$
parameter: t_p = 80 µs,
$V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$



Drain-source on-resistance

$R_{DS\ (on)} = f(T_j)$

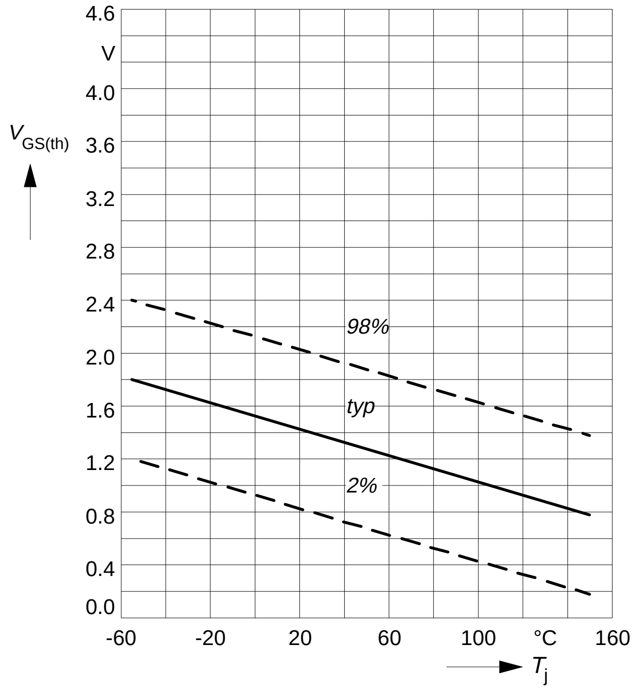
parameter: I_D = 0.2 A, V_{GS} = 10 V



Gate threshold voltage

$V_{GS\ (th)} = f(T_j)$

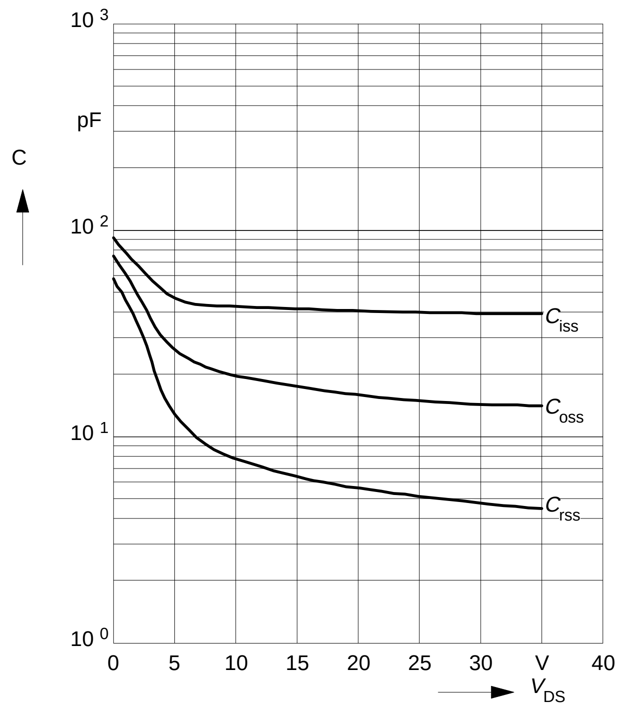
parameter: $V_{GS} = V_{DS}$, I_D = 1 mA



Typ. capacitances

$C = f(V_{DS})$

parameter: V_{GS}=0V, f = 1 MHz



Forward characteristics of reverse diode

$I_F = f(V_{SD})$

parameter: T_j, t_p = 80 µs